Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 10188

M.E./M.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2019.

Second Semester

Applied Electronics

AP 5291 — HARDWARE – SOFTWARE CO-DESIGN

(Common to M.E. Electronics and Communication Engineering/M.E.VLSI Design)

(Regulation 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Classify hardware/software co-design approaches.

2. Identify the requirements of embedded system specification.

3. State the importance of optimisation in HW/SW partitioning problems.

4. How is hardware/software costing estimation carried out?

5. What is hardware/software co-synthesis?

6. Write the significance of state transition graph in hardware/software co-synthesis.

7. Specify the steps involved in high-level synthesis.

8. What is emulation of a system?

9. Identify the various situations that can be covered by concurrency abstraction.

10. Differentiate homogeneous and heterogeneous specifications of a system.

PART B — (5 × 13 = 65 marks)

11. (a) Elaborate the co-design mechanism for heterogeneous implementation of a system.

Or

(b) Discuss an example of a system using multi-processor architectures.

12. (a) Explain in detail how hardware/software partitioning can be done using Genetic algorithms.

Or

(b) Explain hardware/software partitioning using heuristic scheduling.

13. (a) Discuss about the co-synthesis algorithm for distributed system and highlight their characteristic features.

Or

(b) Explain the use of state-transition graph in the hardware/software cosynthesis, with a suitable example.

14. (a) Outline the various emulation systems available for prototyping a system.

Or

(b) Illustrate the suitable architectures for high-performance control applications.

15. (a) Specify the orthogonal dimensions of classifying coordination mechanisms and explain each one of them in detail.

Or

(b) Explain a typical C-VHDL based co-design method with a suitable example.

PART C — (1 × 15 = 15 marks)

16. (a) Consider a system that takes two 16-bit values and produces the GCD of the inputs using Euclid's gcd algorithm. Deduce the following components for the above mentioned system.

- VHDL model
- Intermediate flowgraph
- Circuit
- Controller Graph.

Or

(b) Assume that a unit (the caller) wants to make a call to another (the called). Before starting, reply must be FALSE to indicate that the arbiter is idle. The caller then sets req = alloc and presents the unit numbers of the caller and the called units. If a buffer is available and the called unit is not busy, the arbiter gives a grant by setting reply TRUE, and but is set to the allocated buffer number. Then both of the two units acknowledge receipt of the buffer number. First, the called unit sets req = half, and thereafter the caller sets req = none. Finally, the arbiter sets reply to FALSE. If no buffer is free, the arbiter will respond with reply = TRUE, but = 0 and the called and the caller will have to acknowledge before the arbiter can remove the answer. When the caller wants to release its buffer (hang up), again the 5-phase protocol applies, but the caller uses req = dealloc, and the arbiter responds with the buffer number being released. Specify the above interface and formalize it with a protocol.
