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Question Paper Code : 10187

M.E./M.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2019.

Second Semester

Applied Electronics

AP 5252 — ASIC AND FPGA DESIGN

(Common to M.E. Electronics and Communication Engineering)

(Regulation 2017)

Time : Three hours — Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What are the features of structured gate array?
2. List the sequence of steps to design an ASIC.
3. Name the partitioning methods used in ASIC design.
4. Name the nets, that require special routing.
5. Draw the hierarchy of EDIF.
6. Find the test vector to find the stuck-at-0 fault at output of two input AND gate.
7. What is the function of BIDI in FPGA?
8. Design two input XOR gate using Actel 1 logic module.
9. What are the steps in system level design in the SoC design flow?
10. Represent 011_2 in canonic signed digit arithmetic form.

PART B — (5 × 13 = 65 marks)

11. (a) Briefly explain about FAMOS and SRAM based interconnects.

Or

(b) Compare CPLD and FPGA architectures.

12. (a) Use KL algorithm to partition the circuit in Fig. 1.

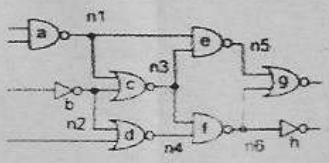

Fig.1

Or

(b) Use Lee Maze algorithm to connect terminals p and q in Fig. 2.

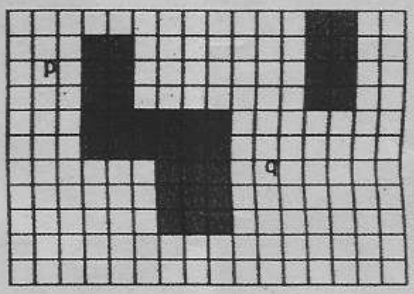

Fig. 2

13. (a) Briefly explain about FSM synthesis in Verilog, with an example.

Or

(b) Explain the boundary scan test procedure used in VLSI systems.

14. (a) Explain any one placement and routing procedure used in FPGA design.

Or

(b) Explain about Data path synthesis and register transfer logic synthesis used in FPGA design.

15. (a) Explain the design of IP based SoC.

Or

(b) Write notes on :

(i) Distributed Arithmetic applied to filter design.

(ii) Bus – based communication architectures.

PART C — (1 × 15 = 15 marks)

16. (a) (i) Find the input to detect stuck-at-1 fault at w10 using ATPG in Fig.3. (8)

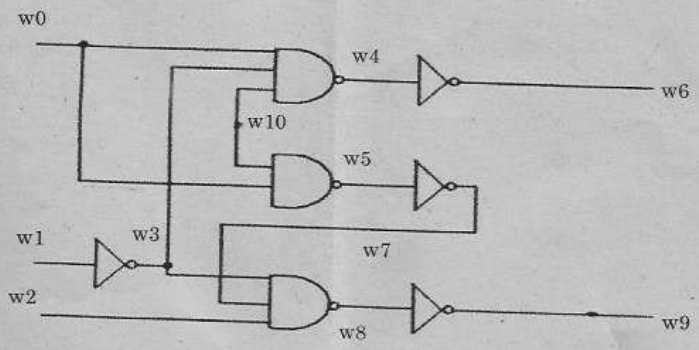

Fig. 3

(ii) Explain the synthesis of a sequential logic circuit using an appropriate example. (7)

Or

(b) Explain the design of digital filters for sigma – delta ADC.