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Question Paper Code : 10183

M.E./M.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2019.

First Semester

Applied Electronics

AP 5151 — ADVANCED DIGITAL SYSTEM DESIGN

(Common to M.E. VLSI Design)

(Regulation 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Write down the steps involved in the design of a CSSN to recognize 0110101/1001010 sequence. Explain.

2. What are the basic building blocks of an ASM chart?

3. What are essential hazards? Give an example.

4. List the objectives of data synchronizers.

5. Recall any two striking attributes of Boolean difference method.

6. Enumerate the steps on Built – in self-test. List its advantages.

7. Compare and contrast the PLA and PAL.

8. Which programming technology is used in Xilmx 4000 series FPGA?

9. How is the compilation of VHDL Code carried out? Summarize.

10. Write a VHDL code to describe a 2 × I multiplexer using behavior model. Explain.

PART B — (5 × 13 = 65 marks)

11. (a) (i) What is an iterative circuit? With an example, enumerate in detail about the design of iterative circuits. (6)

(ii) List and explain the factors influencing the modeling of clocked synchronous sequential networks. (7)

Or

(b) Design a serial adder using mealy model and moore model. Also recall the ASM chart for both the model.

12. (a) Design a asynchronous sequential circuit that has two inputs X_2 and X_1 and one output Z. When $X_1 = 0$ the output Z is 0. The first change in X_2 that occurs while X_1 is 1 will cause Output Z to be 1. The output Z remains at 1 until X_1 returns to be 0. Explain.

Or

(b) (i) Illustrate the mixed operating mode asynchronous sequential circuit with a suitable example. (6)

(ii) Design and digitally construct a fully operational vending machine which should be flexible enough to allow for multiple programming modes and it should be reliable and user-friendly. Explain. (7)

13. (a) (i) Explain the algorithm to find fault in logic circuit with an example. (6)

(ii) With an illustration, discuss in detail about the Boolean difference method. Show its uses with an example. (7)

Or

(b) Write short notes on the following testing procedure for PLAs

(i) Tolerance techniques (6)

(ii) DFT schemes. Show how they are different from one another. (7)

14. (a) Design and demonstrate a 4 bit serial-in, serial-out shift register and implement it using suitable sequential PAL.

Or

(b) Explain in detail about the CLB and the I/O block of a Xilinx 4000 series FGPA.

15. (a) What is Structural modeling? Write a VHDL code to realize a 4-bit parallel adder using structural modeling and enumerate it using a flow chart.

Or

(b) Explain the different data types and operators used for modelling in Verilog.

PART C — (1 × 15 = 15 marks)

16. (a) (i) Estimate the minimum state equivalent of the state table given. (7)

Present state	Next State/Output	
	Input x = 0	Input x = 1
q_0	$q_0/1$	$q_4/0$
q_1	$q_0/0$	$q_4/0$
q_2	$q_1/0$	$q_5/0$
q_3	$q_1/0$	$q_5/0$
q_4	$q_2/0$	$q_6/0$
q_5	$q_2/0$	$q_6/0$
q_6	$q_3/0$	$q_7/0$
q_7	$q_3/0$	$q_7/0$

(ii) Construct a VHDL code to realize a 3 × 3 multiplier and a test bench to test its functionality. (8)

Or

(b) (i) Discuss whether the following state table contains essential hazards are not. (7)

Present state	Next State		Output Z
	Input X = 0	Input X = 1	
A	A	B	0
B	B	C	0
C	C	D	0
D	D	A	1

(ii) Construct a VHDL Code for Binary Multiplier and Binary Divider. (8)

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